Claims

1. An operational amplifier (op-amp) configurable in a non-inverting mode with a closed loop gain greater than one, and with correction in an output signal of the op-amp for a time varying voltage reference of the op-amp relative to a true voltage reference, the op-amp comprising:

a primary output for providing the output signal gained up from an input signal,

a primary differential input amplifier stage operable with a transconductance and having a non-inverting input defining a primary non-inverting input of the op-amp for receiving the input signal, an inverting input defining a primary inverting input of the op-amp for coupling to a feedback loop from the primary output, and an output for providing an intermediate current signal from which the output signal on the primary output is derived, and

a secondary differential input amplifier stage operable with a transconductance, and responsive to the time varying voltage reference for providing a secondary current signal responsive to variation in the time varying voltage reference relative to the true voltage reference for summing with the intermediate current signal provided by the primary differential input amplifier stage, the transconductance of the secondary differential input amplifier stage being a function of the transconductance of the primary differential input amplifier stage, so that the output signal on the primary output derived from the sum of the intermediate and secondary currents includes correction for the time varying voltage reference.

2. An op-amp as claimed in Claim 1 in which the secondary differential input amplifier stage comprises a non-inverting input for coupling to the time varying voltage reference, and an inverting input for coupling to the true voltage reference.

3. An op-amp as claimed in Claim 1 in which the secondary differential input amplifier stage comprises an output for providing the secondary current signal, the output of the secondary differential input amplifier stage being coupled to the output of the primary differential input amplifier stage.

4. An op-amp as claimed in Claim 1 in which the transconductance of the secondary differential input amplifier stage is a function of the closed loop gain of the op-amp and the transconductance of the primary differential input amplifier stage.

5. An op-amp as claimed in Claim 1 in which the transconductance of the secondary differential input amplifier stage is substantially equal to the transconductance of the primary differential input amplifier stage less the quotient of the transconductance of the primary differential input amplifier stage divided by the closed loop gain of the op-amp.

6. An op-amp as claimed in Claim 1 in which the op-amp is configured with a closed loop gain greater than one, and a feedback loop comprising a first impedance element is provided coupling the primary output and the primary inverting input of the op-amp, a second impedance element being provided for coupling the primary inverting input with the time varying voltage reference, the second impedance element co-operating with the first impedance element for setting the closed loop gain of the op-amp.

7. An op-amp as claimed in Claim 6 in which the ratio of the impedance of the first impedance element to the impedance of the second impedance element is approximately 1.

8. An op-amp as claimed in Claim 6 in which each of the first and second impedance elements are resistive elements.

9. An op-amp as claimed in Claim 1 in which the primary differential input stage of the op-amp comprises:

a first differential pair having a first transistor, a gate of which defines the primary non-inverting input, and a second transistor, a gate of which defines the primary inverting input,

a first current mirror circuit coupled to the first differential pair and defining with the first transistor a first node, and with the inverting transistor a second node, the first node defining the output of the primary differential input amplifier stage, and

a first constant current source for providing a constant current to the first differential pair.

10. An op-amp as claimed in Claim 9 in which the secondary differential input amplifier stage comprises:

a second differential pair having a third transistor, a gate of which defines the non-inverting input of the secondary differential input amplifier stage, and a fourth transistor, a gate of which defines the inverting input of the secondary differential input amplifier stage, the differential pair being coupled to a current mirror circuit, which defines with the third transistor a third node, and with the fourth transistor a fourth node, the third node defining the output of the secondary differential input amplifier stage, and being coupled to the first node of the primary differential input amplifier stage, and

a second constant current source for providing a constant current to the second differential amplifier pair.

11. An op-amp as claimed in Claim 10 in which the fourth node of the secondary differential input amplifier stage is coupled to the second node of the primary differential input amplifier stage.

12. An op-amp as claimed in Claim 10 in which the current mirror circuit to which the second differential pair is coupled is the first current mirror circuit of the primary differential input amplifier stage.

13. An op-amp as claimed in Claim 1 in which the op-amp is implemented as an integrated circuit by a CMOS process.

14. An op-amp configured in a non-inverting mode with a closed loop gain greater than one, and referenced to a time varying voltage reference relative to a true voltage reference, with correction in an output signal of the op-amp for the time varying voltage reference, the op-amp comprising:

a primary output for providing the output signal gained up from a corresponding input signal,

a primary differential input amplifier stage operable with a transconductance and having a non-inverting input defining a primary non-inverting input of the op-amp for receiving the corresponding input signal, an inverting input defining a primary inverting input of the op-amp, and an output for providing an intermediate current signal from which the output signal on the corresponding primary output is derived,

a feedback loop coupling the primary output with the primary inverting input,

a secondary differential input amplifier stage operable with a transconductance, and responsive to the time varying voltage reference for providing a secondary current signal responsive to variation in the time varying voltage reference relative to the true voltage reference for summing with the intermediate current signal provided by the primary differential input amplifier stage, the transconductance of the secondary differential input amplifier stage of the op-amp being a function of the transconductance of the primary differential input amplifier stage of the op-amp, so that the output signal on the primary output of the op-amp, which is derived from the sum of the corresponding intermediate and secondary currents includes correction for the time varying voltage reference.

15. An op-amp as claimed in Claim 14 in which the feedback loop comprising a first impedance element, and a second impedance element is provided for coupling the primary inverting input with the time varying voltage reference, the second impedance element co-operating with the first impedance element for setting the closed loop gain of the op-amp.

16. An op-amp as claimed in Claim 15 in which each of the first and second impedance elements are resistive elements.

17. A circuit comprising a plurality of op-amps, each op-amp being configured in a non-inverting mode with a closed loop gain greater than one, and referenced to a time varying voltage reference relative to a true voltage reference, with correction in an output signal of each op-amp for the time varying voltage reference, each op-amp comprising:

a primary output for providing the output signal gained up from a corresponding input signal,

a primary differential input amplifier stage operable with a transconductance and having a non-inverting input defining a primary non-inverting input of the op-amp for receiving the corresponding input signal, an inverting input defining a primary inverting input of the op-amp, and an output for providing an intermediate current signal from which the output signal on the corresponding primary output is derived,

a feedback loop coupling the primary output with the primary inverting input,

a secondary differential input amplifier stage operable with a transconductance, and responsive to the time varying voltage reference for providing a secondary current signal responsive to variation in the time varying voltage reference relative to the true voltage reference for summing with the intermediate current signal provided by the primary differential input amplifier stage, the transconductance of the secondary differential input amplifier stage of each op-amp being a function of the transconductance of the primary differential input amplifier stage of the corresponding op-amp, so that the output signal on the primary output of the corresponding op-amp, which is derived from the sum of the corresponding intermediate and secondary currents includes correction for the time varying voltage reference.

18. A circuit as claimed in Claim 17 in which a plurality of digital-to-analog converters are provided corresponding the respective op-amps, each digital-to-analog converter having an analog output for outputting an analog signal corresponding to a respective digital input word, the analog output of each digital-to-analog converter being coupled to the primary non-inverting input of the corresponding op-amp, so that the output signal provided by each op-amp is gained up from the analog signal of the corresponding digital-to-analog converter with correction for the time varying voltage reference.

19. A circuit as claimed in Claim 17 in which a common voltage reference rail is provided, and the op-amps are referenced to the common voltage reference rail, the common voltage reference rail being coupled to the true voltage reference through a coupling means having inherent impedance, so that as the output signals through the primary outputs of the respective op-amps vary in response to variation in the corresponding input signals, current through the coupling means varies, thereby inducing the time varying voltage reference in the common voltage reference rail.

20. A circuit as claimed in Claim 17 in which the circuit is implemented as an integrated circuit by a CMOS process, the circuit comprising a voltage reference pin to which the true voltage reference is applied.

21. A method for providing correction in an output signal of an op-amp, configured in a non-inverting mode with a closed loop gain greater than one, for a time varying voltage reference of the op-amp relative to a true voltage reference, the op-amp comprising a primary output for providing the output signal gained up from an input signal, and a primary differential input amplifier stage operable with a transconductance and having a non-inverting input defining a primary non-inverting input of the op-amp for receiving the input signal, an inverting input defining a primary inverting input of the op-amp for coupling to a feedback loop from the primary output, and an output for providing an intermediate current signal from

which the output signal on the primary output is derived, the method comprising the steps of:

providing a secondary differential input amplifier stage operable with a transconductance, and responsive to the time varying voltage reference for providing a secondary current signal responsive to variation in the time varying voltage reference relative to the true voltage reference for summing with the intermediate current signal provided by the primary differential input amplifier stage, and

selecting the transconductance of the secondary differential input amplifier stage to be a function of the transconductance of the primary differential input amplifier stage, so that the output signal on the primary output derived from the sum of the intermediate and secondary currents includes correction for the time varying voltage reference.

22. A method as claimed in Claim 21 in which the secondary differential input amplifier stage is provided with a non-inverting input, an inverting input and an output, and the method further comprises coupling the non-inverting input of the secondary differential input amplifier stage to the time varying voltage reference, coupling the inverting input of the secondary differential input amplifier stage to the true voltage reference, and coupling the output of the secondary differential input amplifier stage to the output of the primary differential input amplifier stage for summing the secondary current signal responsive to the time varying voltage reference through the output of the secondary differential input amplifier stage with the intermediate current signal through the output of the primary differential input amplifier stage.

23. A method as claimed in Claim 21 in which the transconductance of the secondary differential input amplifier stage is selected to be a function of the closed loop gain of the op-amp and the transconductance of the primary differential input amplifier stage.

24. A method as claimed in Claim 21 in which the transconductance of the secondary differential input amplifier stage is selected to be substantially equal to the transconductance of the primary differential input amplifier stage less the quotient of the transconductance of the primary differential input amplifier stage divided by the closed loop gain of the op-amp.

25. A method as claimed in Claim 21 in which the feedback loop is provided and comprises a first impedance element coupled to the primary output and the primary inverting input of the op-amp, and a second impedance element couples the primary inverting input of the op-amp with the time varying voltage reference, the second impedance element co-operating with the first impedance element for setting the closed loop gain of the op-amp.

26. A method as claimed in Claim 25 in which the ratio of the impedance of the first impedance element to the impedance of the second impedance element is approximately one.

27. A method as claimed in Claim 25 in which each of the first and second impedance elements are resistive elements.